AN ULTRA-HIGH SPEED DCFL DYNAMIC FREQUENCY DIVIDER

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ABSTRACT

A new circuit of a DCFL (Direct Coupled FET Logic) dynamic frequency divider has been developed using 0.25μm gate inverted HEMTs. The divider is operated with a single signal input in a very wide frequency range from 1.8GHz to 15GHz with low power dissipation of 62mW. The maximum operating frequency of 26.5GHz is obtained.

INTRODUCTION

A frequency divider with high speed and low power dissipation is required for the phase locked loop used in microwave systems. For that purpose, dynamic dividers have been extensively developed [1][2][3][4] because of an advantage of its small propagation delay time for the critical path. In such dynamic divider circuits, a dual-phase input signal is generally used to expand an operating frequency range. However, that makes a system design complex and the operation of the divider becomes unstable due to the phase difference between the two input signals. To avoide such a problem, the input buffer circuit is generally used to supply a dual-phase signal for the dynamic divider despite of the complexity of circuit design.

We propose a new circuit of a DCFL dynamic frequency divider which operates with a single signal input. In this circuit, a latch is used to guarantee its operation especially at a low frequency. Moreover, using DCFL as a basic logic gate and the circuit configuration where the latch does not form a critical path, the circuit has realized a high speed operation at a very low power dissipation. In addition, DCFL needs only one supply voltage, which is an advantage for the system design.

In this paper, we report the circuit design and the performance of the new dynamic frequency divider which operates with a single signal-input, high speed, low power dissipation and a wide frequency range, implemented by 0.25μm gate inverted HEMTs (I-HEMTs).

CIRCUIT DESIGN

Fig.1 shows a schematic circuit diagram of the binary dynamic frequency divider. The circuit consists of two transmission gates, cross-coupled inverters and buffers. The cross-coupled inverters work as a latch. The buffers are used to drive the next gate and obtain an adequate delay time. The cross-coupled inverters and buffers consist of DCFL configuration. The transmission gates consist of E-FETs. The gate width of E-FETs is 24μm for the transmission gates, 48μm for buffers and 10μm for cross coupled inverters. The threshold voltage designed is 100mV for E-FET and -500mV for D-FET.

The operation of the dynamic divider is as follows. "c" is an input signal applied to transmission gates. During the logic level of "c" is "low", the transmission gates are closed. The logic level of the input of the buffers is maintained by a latch. Output signals of the buffers, of which logic level is opposite to that of a latch, are transferred to transmission gates through feedback loops. During the next half cycle of an input signal, the logic level of "c" becomes "high" and transmission gates open. The output signals of buffers are transferred to a latch and buffers, then, the logic levels of a latch and buffers are turned over. In the next half cycle, the logic level of "c" becomes "low" and

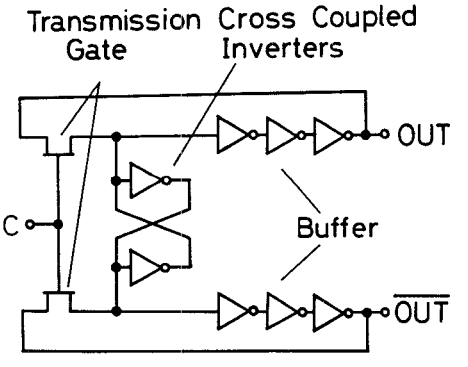

Fig.1. Binary dynamic frequency divider circuit.

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transmission gates are closed before the opposite signals from buffers are transferred to the transmission gates. Therefore the logic level is not changed, and input frequency is divided.

In this circuit, the output level of a latch and the input of buffers are fixed at the same time. The latch does not form a critical path, which results the small propagation delay time. For a correct operation, the gate width of the latch is designed smaller than that of buffers, which is advantageous for a reduction of a fan-out load in the critical path.

The condition for correct operation is given by

$$\tau_{TF} < \tau_{IN-H} < \tau_{LPD} \qquad (1)$$

where

$$\tau_{LPD} = \tau_{TF} + n\tau_{B} \qquad (2)$$

τ_{IN-H} is the period of the "high" level of the input signal, τ_{LPD} is the total propagation delay time, τ_{TF} is a delay time of a transmission gate and τ_{B} is that of a buffer inverter. "n" is the number of buffers and in this study it is determined to be 3 as shown in Fig. 1. The circuit has no limitations on a low level period of an input signal, which is great advantageous for low frequency operation.

The total propagation delay time mainly determines the operating frequency range of a dynamic divider. As the delay time decreases, the operating frequency range shifts to a higher region. The maximum input frequency ,fop-max, and the minimum input frequency, fop-min, is given by

$$\text{fop-max} = 1 / \tau_{LPD} \quad \text{for } a \geq \tau_{TF}/\tau_{LPD} \qquad (3)$$

$$\text{fop-max} = a / \tau_{TF} \quad \text{for } a \leq \tau_{TF}/\tau_{LPD} \qquad (4)$$

$$\text{fop-min} = a / \tau_{LPD} \qquad (5)$$

where

$$a = \tau_{IN-H}/\tau_{IN} \qquad (6)$$

τ_{IN} is a period of an input signal and "a" is the ratio of the period of high level to τ_{IN}.

From the Eq.5, as the ratio "a" decreases, fop-min become small. Therefore, the divider is able to operate statically, from DC, when the period of high level for input signal is constant independent of the input frequency.

To evaluate the performances of the binary dynamic frequeny divider, a 1/8 frequency divider, whose logic diagram is shown in Fig.2, was designed. The 1/8 divider consists of the dynamic divider described above as the first stage, two DCFL static dividers and output buffers connected to 50Ω. The dynamic divider can be directly

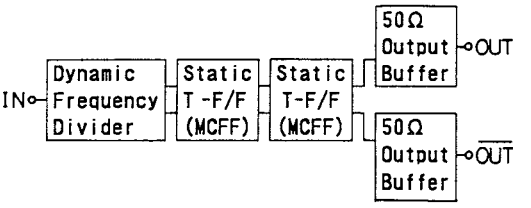

Fig.2. Block diagram of a 1/8 frequency divider.

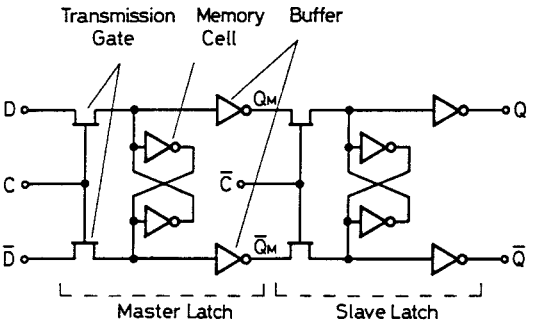

Fig.3. Schematic diagram of MCFF.

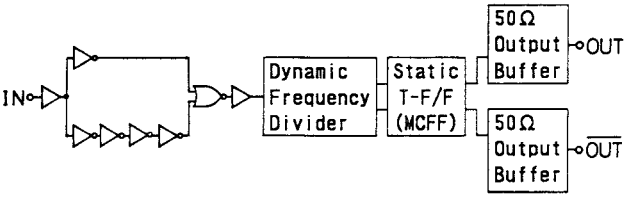

Fig.4. Block diagram of a 1/4 frequency divider with an input buffer.

connected to the DCFL circuits. Output buffers are composed of SBFL (Supper Buffered FET Logic). The DCFL static dividers are composed of MCFF(Memory Cell type Flip Flop)[6]. The schematic circuit diagram of MCFF is shown in Fig.3. The operating frequency range is wide enough to evaluate the performance of a dynamic divider. The maximum toggle frequency of 16GHz for a static divider and the maximum data bit rate of over 10GHz for a D-FF was already reported for the circuits implemented by 0.5μm gate length GaAs MESFETs.

To evaluate the possibility of DC operation, a 1/4 dynamic divider with an input buffer was designed. The schematic circuit diagram is shown in Fig.4. The input buffer generates the pulse of high level whose duration is held constant independent of input frequency.

FABRICATION PROCESS

The divider ICs were implemented by 0.25μm gate I-HEMTs which had an advantage of the small

Table 1. Characteristics of FETs

Mode	Vth (mV)	g_m(mS/mm)	K-value(mA/mmV²)
E-FET	83	321	363
D-FET	-523	187	210

short channel effect[6]. The fabrication process of I-HEMT is as follows. The inverted HEMT structure was grown by a conventional Ⅲ-Ⅴ MBE system on a 2-inch HB semi-insulating GaAs wafer. Active layers were isolated by oxygen ion implantation. The gate recess was performed by RIBE using an electron-cyclotron resonance(ECR) plasma. An etching gas was Cl_2 and an acceleration voltage was 200V. A deep-UV photoresist was used as an etching mask. After the recess etching, Al metal was evaporated and patterned by the lift-off technique. AuGe/Ni/Au was used for source and drain ohmic contact. The threshold voltage of fabricated I-HEMTs was 83.4mV for E-FET and was -523mV for D-FET. The parameters of fabricated I-HEMTs are shown in Table 1, where the transconductance was measured at Vgs=0.6V for E-FET and Vgs=0V for D-FET.

A propagation delay time of 20.6 psec/gate with a power dissipation of 0.97mW/gate was obtained at a supply voltage of 1V.

The microphotograph of the fabricated dynamic divider is shown in Fig.5. The occupied area was 92X128 μm.

EXPERIMENTAL RESULTS

For a measurement, the chip was constructed in a ceramic package with its 50Ω signal line.

Fig.6 shows the dependence of the minimum input sensitivity (Vp-p) of the 1/8 divider on the operating frequency at a supply voltage of 1V. The divider operated in the frequency range from 1.8GHz to 15GHz. The power dissipation of the 1/8 divider was 62 mW without output buffers. The part of 1/2 dynamic divider in Fig.2 was estimated to dissipate 16.3mW from the gate width. The maximum frequency of 15GHz is in good agreement with the estimation from Eq.3 for obtained delay time of DCFL inverters. The minimum frequency of 1.8GHz is satisfactorily estimated from Eq.5 when transmission gates open during about 10% of input signal period.

Fig.7 shows the dependence of the maximum operating frequency and the power dissipation of 1/8 divider on the supply voltage. A maximum operating frequency of 26.5GHz was obtained when the supply voltage was increased up to 5V. An input waveform of 26.5GHz and an output of the 1/8 divider are shown in Fig.8.

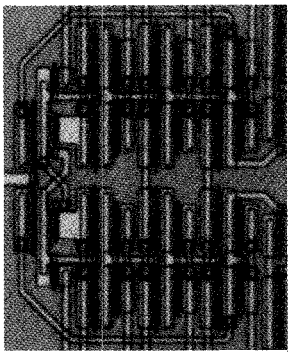

Fig.5. Microphotograph of a fabricated dynamic divider.

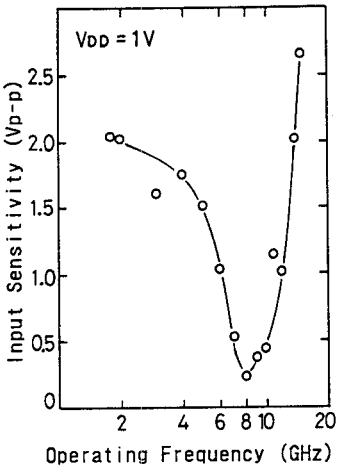

Fig.6. The dependence of the input sensitivity (Vp-p) of a 1/8 frequency divider on the operating frequency at a supply voltage of 1V.

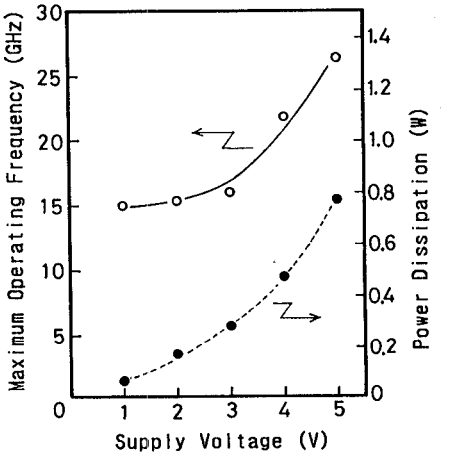

Fig.7. The dependence of the maximum operating frequency and the power dissipation of a 1/8 frequency divider on the supply voltage.

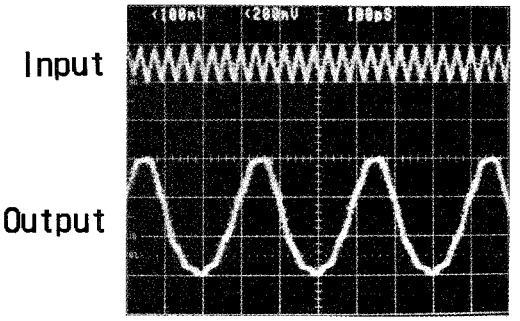

Fig.8. An input waveform of 26.5GHz and an output of a 1/8 frequency divider.

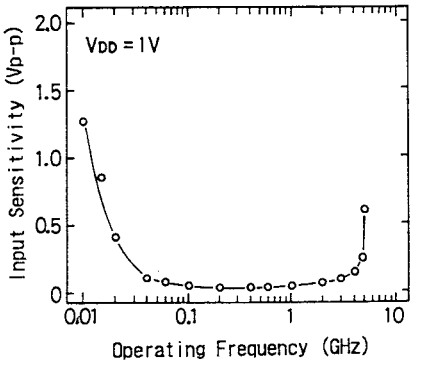

Fig.9. The dependence of the input sensitivity (Vp-p) of a 1/4 frequency divider with an input buffer on the operating frequency at a supply voltage of 1V.

Fig.9 shows the dependence of an input sensitivity of a 1/4 dynamic divider with an input buffer on the operating frequency at a supply voltage of 1V. An operating frequency of as small as 10MHz was confirmed with the maximum operating frequency of 5.0GHz. The input and output waveforms at 10MHz is shown in Fig.10. The result demonstrates that the dynamic divider is able to operate from a very low frequency.

CONCLUSION

A new circuit of DCFL dynamic frequency divider is proposed and a 1/8 divider was developed using 0.25μm gate I-HEMTs. It is proved that the divider operates with single input signal in a very wide frequency range from 1.8GHz to 15GHz with a power dissipation of as small as 62mW. The maximum operating frequency was 26.5GHz, which is the best result ever reported for DCFL circuits. These results indicate that the dynamic frequency divider newly developed is applicable up to millimeter wave region for the microwave systems.

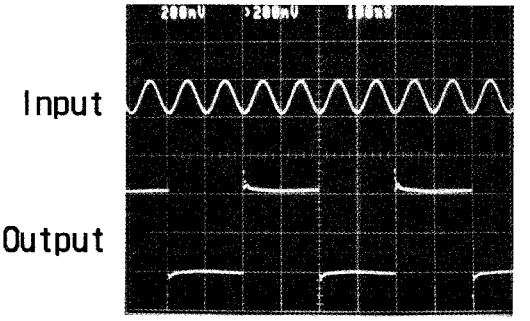

Fig.10. An input waveform of 10MHz and an output of a 1/4 frequency divider.

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